

## WHAT IS CLAIMED IS:

- 1 1. An apparatus having a transfer mode abnormality  
2 detecting function comprising:  
3           at least two modules connected to each other  
4 through an interface bus in at least two different  
5 modes so that data can be transferred between said  
6 modules;  
7           a determining means for determining whether  
8 or not a basic mode predetermined between said at least  
9 two different modes agrees with a mode set in a mode  
10 setting sequence executed when said apparatus is reset  
11 or when data is transferred between said modules; and  
12           a notifying means for determining that  
13 transfer mode abnormality occurs when said  
14 determining means determines that said modes do not  
15 agree with each other, and for notifying of an error  
16 notice.
- 1 2. The apparatus having a transfer mode abnormality  
2 detecting function according to claim 1 further  
3 comprising:  
4           a controlling means for rerunning said mode  
5 setting sequence in response to said error notice from  
6 said notifying means.
- 1 3. The apparatus having a transfer mode abnormality

2 detecting function according to claim 2, wherein when  
3 said determining means again determines that said  
4 modes do not agree with each other after said  
5 controlling means reruns said mode setting sequence,  
6 said notifying means determines that a failure occurs  
7 and notifies of a failure notice.

1 4. The apparatus having a transfer mode abnormality  
2 detecting function according to claim 1, wherein said  
3 determining means determines that said modes do not  
4 agree with each other when a confirmation signal  
5 responding to said basic mode remains disabled at the  
6 time of executing said mode setting sequence.

1 5. The apparatus having a transfer mode abnormality  
2 detecting function according to claim 1, wherein said  
3 interface bus is a PCI (Peripheral Component  
4 Interconnect) bus.

1 6. The apparatus having a transfer mode abnormality  
2 detecting function according to claim 2, wherein said  
3 interface bus is a PCI (Peripheral Component  
4 Interconnect) bus.

1 7. The apparatus having a transfer mode abnormality  
2 detecting function according to claim 3, wherein said  
3 interface bus is a PCI (Peripheral Component

4 Interconnect) bus.

1 8. The apparatus having a transfer mode abnormality  
2 detecting function according to claim 4, wherein said  
3 interface bus is a PCI (Peripheral Component  
4 Interconnect) bus.

1 9. The apparatus having a transfer mode abnormality  
2 detecting function according to claim 5, wherein said  
3 interface bus is a 64-bit PCI bus, said at least two  
4 different modes are a 64-bit transfer mode and a 32-bit  
5 transfer mode, said basic mode is said 64-bit transfer  
6 mode; and  
7           when said determining means determines that  
8 said modes do not agree with each other, said notifying  
9 means determines that an inefficient transfer status  
10 occurs as said transfer mode abnormality, and notifies  
11 of said error notice.

1 10. The apparatus having a transfer mode abnormality  
2 detecting function according to claim 6, wherein said  
3 interface bus is a 64-bit PCI bus, said at least two  
4 different modes are a 64-bit transfer mode and a 32-bit  
5 transfer mode, said basic mode is said 64-bit transfer  
6 mode; and  
7           when said determining means determines that  
8 said modes do not agree with each other, said notifying

9 means determines that an inefficient transfer status  
10 occurs as said transfer mode abnormality, and notifies  
11 of said error notice.

1 11. The apparatus having a transfer mode abnormality  
2 detecting function according to claim 7, wherein said  
3 interface bus is a 64-bit PCI bus, said at least two  
4 different modes are a 64-bit transfer mode and a 32-bit  
5 transfer mode, said basic mode is said 64-bit transfer  
6 mode; and

7           when said determining means determines that  
8 said modes do not agree with each other, said notifying  
9 means determines that an inefficient transfer status  
10 occurs as said transfer mode abnormality, and notifies  
11 of said error notice.

1 12. The apparatus having a transfer mode abnormality  
2 detecting function according to claim 8, wherein said  
3 interface bus is a 64-bit PCI bus, said at least two  
4 different modes are a 64-bit transfer mode and a 32-bit  
5 transfer mode, said basic mode is said 64-bit transfer  
6 mode; and

7           when said determining means determines that  
8 said modes do not agree with each other, said notifying  
9 means determines that an inefficient transfer status  
10 occurs as said transfer mode abnormality, and notifies  
11 of said error notice.

1 13. A storage controlling apparatus disposed between  
2 a disk unit and a host to control an access from said  
3 host to said unit, said storage controlling apparatus  
4 comprising:

5           a disk interface module for controlling an  
6 interface with said disk unit;

7           a host interface module for controlling an  
8 interface with said host;

9           a management module for generally managing  
10 the whole of said apparatus;

11           a bridge module connected said disk interface  
12 module, said host interface module and said management  
13 module through interface buses to connect said disk  
14 interface module, said host interface module and said  
15 management module to one another so that data can be  
16 transferred among said disk interface module, said  
17 host interface module and said management module;

18           said disk interface module, said host  
19 interface module, said management module and said  
20 bridge module being connected in at least two  
21 different modes so that data can be transferred among  
22 said disk interface module, said host interface module,  
23 said management module and said bridge module;

24           a determining means for determining whether  
25 or not a basic mode predetermined between said at least  
26 two different modes agrees with a mode set in a mode

27 setting sequence executed when said storage  
28 controlling apparatus is reset or when data is  
29 transferred among said modules; and

30 a notifying means for determining that  
31 transfer mode abnormality occurs when said  
32 determining means determines that said modes do not  
33 agree with each other, and for notifying of an error  
34 notice.

1 14. The storage controlling apparatus according to  
2 claim 13 further comprising:

3 a controlling means for rerunning said mode  
4 setting sequence when receiving said error notice from  
5 said notifying means.

1 15. The storage controlling apparatus according to  
2 claim 14, wherein when said determining means again  
3 determines that said modes do not agree with each other  
4 after said controlling means reruns said mode setting  
5 sequence, said notifying means determines that a  
6 failure occurs and notifies of a failure notice.

1 16. The storage controlling apparatus according to  
2 claim 13, wherein said determining means determines  
3 that said modes do not agree with each other when a  
4 confirmation signal responding to said basic mode  
5 remains disabled at the time of executing said mode

6    setting sequence.

1    17. The storage controlling apparatus according to  
2    claim 13, wherein said interface buses are PCI  
3    (Peripheral Component Interconnect) buses.

1    18. The storage controlling apparatus according to  
2    claim 14, wherein said interface buses are PCI  
3    (Peripheral Component Interconnect) buses.

1    19. The storage controlling apparatus according to  
2    claim 15, wherein said interface buses are PCI  
3    (Peripheral Component Interconnect) buses.

1    20. The storage controlling apparatus according to  
2    claim 16, wherein said interface buses are PCI  
3    (Peripheral Component Interconnect) buses.

1    21. The storage controlling apparatus according to  
2    claim 17, wherein said interface buses are 64-bit PCI  
3    buses, said at least two different modes are a 64-bit  
4    transfer mode and a 32-bit transfer mode, said basic  
5    mode is said 64-bit transfer mode; and

6                when said determining means determines that  
7    said modes do not agree with each other, said notifying  
8    means determines that an inefficient transfer status  
9    occurs as said transfer mode abnormality, and notifies

10 of said error notice.

1 22. The storage controlling apparatus according to  
2 claim 18, wherein said interface buses are 64-bit PCI  
3 buses, said at least two different modes are a 64-bit  
4 transfer mode and a 32-bit transfer mode, said basic  
5 mode is said 64-bit transfer mode; and

6 when said determining means determines that  
7 said modes do not agree with each other, said notifying  
8 means determines that an inefficient transfer status  
9 occurs as said transfer mode abnormality, and notifies  
10 of said error notice.

1 23. The storage controlling apparatus according to  
2 claim 19, wherein said interface buses are 64-bit PCI  
3 buses, said at least two different modes are a 64-bit  
4 transfer mode and a 32-bit transfer mode, said basic  
5 mode is said 64-bit transfer mode; and

6 when said determining means determines that  
7 said modes do not agree with each other, said notifying  
8 means determines that an inefficient transfer status  
9 occurs as said transfer mode abnormality, and notifies  
10 of said error notice.

1 24. The storage controlling apparatus according to  
2 claim 20, wherein said interface buses are 64-bit PCI  
3 buses, said at least two different modes are a 64-bit



4 transfer mode and a 32-bit transfer mode, said basic  
5 mode is said 64-bit transfer mode; and  
6 when said determining means determines that  
7 said modes do not agree with each other, said notifying  
8 means determines that an inefficient transfer status  
9 occurs as said transfer mode abnormality, and notifies  
10 of said error notice.

1 25. An interface module for a storage controlling  
2 apparatus disposed between a disk unit and a host to  
3 control an access from said host to said disk unit,  
4 said storage controlling apparatus comprising said  
5 interface module for controlling an interface with  
6 said disk unit or said host, a management module for  
7 generally managing the whole of said storage  
8 controlling apparatus, and a bridge module for  
9 connecting said interface module and said management  
10 module to each other so that data can be transferred  
11 between said interface module and said management  
12 module, said interface module comprising:

13 a first transfer processing unit for  
14 controlling data transfer between said interface  
15 module and said disk unit or said host;

16 a second transfer processing unit for  
17 controlling data transfer between said interface  
18 module and said bridge module;

19 said two transfer processing units being

20 connected to each other in at least two different modes  
21 through an interface bus so that data can be  
22 transferred between said two transfer processing  
23 units;

24 a determining means for determining whether  
25 or not a basic mode predetermined between said at least  
26 two different modes agrees with a mode set in a mode  
27 setting sequence executed when said interface module  
28 is reset or when data is transferred between said two  
29 transfer processing units; and

30 a notifying means for determining that  
31 transfer mode abnormality occurs when said  
32 determining means determines that said modes do not  
33 agree with each other, and for notifying of an error  
34 notice.

1 26. The interface module for a storage controlling  
2 apparatus according to claim 25 further comprising:

3 a controlling means for rerunning said mode  
4 setting sequence when receiving said error notice from  
5 said notifying means.

1 27. The interface module for a storage controlling  
2 apparatus according to claim 26, wherein when said  
3 determining means again determines that said modes do  
4 not agree with each other after said controlling means  
5 reruns said mode setting sequence, said notifying

6 means determines that a failure occurs, and notifies  
7 of a failure notice.

1 28. The interface module for a storage controlling  
2 apparatus according to claim 25, wherein when a  
3 confirmation signal responding to said basic mode  
4 remains disabled at the time of executing said mode  
5 setting sequence, said determining means determines  
6 that said modes do not agree with each other.

1 29. The interface module for a storage controlling  
2 apparatus according to claim 25, wherein said  
3 interface bus is a PCI (Peripheral Component  
4 Interconnect) bus.

1 30. The interface module for a storage controlling  
2 apparatus according to claim 26, wherein said  
3 interface bus is a PCI (Peripheral Component  
4 Interconnect) bus.

1 31. The interface module for a storage controlling  
2 apparatus according to claim 27, wherein said  
3 interface bus is a PCI (Peripheral Component  
4 Interconnect) bus.

1 32. The interface module for a storage controlling  
2 apparatus according to claim 28, wherein said

3 interface bus is a PCI (Peripheral Component  
4 Interconnect) bus.

1 33. The interface module for a storage controlling  
2 apparatus according to claim 29, wherein said  
3 interface bus is a 64-bit PCI bus, said at least two  
4 different modes are a 64-bit transfer mode and a 32-bit  
5 transfer mode, said basic mode is said 64-bit transfer  
6 mode; and  
7           when said determining means determines that  
8 said modes do not agree with each other, said notifying  
9 means determines that an inefficient transfer status  
10 occurs as said transfer mode abnormality, and notifies  
11 of said error notice.

1 34. The interface module for a storage controlling  
2 apparatus according to claim 30, wherein said  
3 interface bus is a 64-bit PCI bus, said at least two  
4 different modes are a 64-bit transfer mode and a 32-bit  
5 transfer mode, said basic mode is said 64-bit transfer  
6 mode; and  
7           when said determining means determines that  
8 said modes do not agree with each other, said notifying  
9 means determines that an inefficient transfer status  
10 occurs as said transfer mode abnormality, and notifies  
11 of said error notice.

1 35. The interface module for a storage controlling  
2 apparatus according to claim 31, wherein said  
3 interface bus is a 64-bit PCI bus, said at least two  
4 different modes are a 64-bit transfer mode and a 32-bit  
5 transfer mode, said basic mode is said 64-bit transfer  
6 mode; and

7           when said determining means determines that  
8 said modes do not agree with each other, said notifying  
9 means determines that an inefficient transfer status  
10 occurs as said transfer mode abnormality, and notifies  
11 of said error notice.

1 36. The interface module for a storage controlling  
2 apparatus according to claim 32, wherein said  
3 interface bus is a 64-bit PCI bus, said at least two  
4 different modes are a 64-bit transfer mode and a 32-bit  
5 transfer mode, said basic mode is said 64-bit transfer  
6 mode; and

7           when said determining means determines that  
8 said modes do not agree with each other, said notifying  
9 means determines that an inefficient transfer status  
10 occurs as said transfer mode abnormality, and notifies  
11 of said error notice.